3 A, Low V_{IN}, Low Noise, CMOS Linear Regulator

Preliminary Technical Data

ADP1763

FEATURES

- 3 A maximum output current
- Low input voltage supply range
  - V_{IN} = 1.10 V to 1.98 V, no external bias supply required
- Fixed output voltage range: V_{OUT_FIXED} = 0.9 V to 1.5 V
- Adjustable output voltage range: V_{OUT_ADJ} = 0.5 V to 1.5 V
- Ultralow noise: 2 µV rms, 100 Hz to 100 kHz
- Noise spectral density
  - 4 nV/√Hz at 10 kHz
  - 3 nV/√Hz at 100 kHz
- Low dropout voltage: 115 mV typical at 3 A load
- Operating supply current: 4.5 mA typical at no load
- −1.8% to +1.5% fixed output voltage accuracy over line, load, and temperature
- Excellent power supply rejection ratio (PSRR) performance
  - 59 dB typical at 10 kHz at 3 A load
  - 43 dB typical at 100 kHz at 3 A load
- Excellent load/line transient response
- Soft start to reduce inrush current
- Optimized for small 10 µF ceramic capacitors
- Current-limit and thermal overload protection
- Power-good indicator
- Precision enable
- 16-lead, 3 mm × 3 mm LFCSP package

APPLICATIONS

- Regulation to noise sensitive applications such as radio frequency (RF) transceivers, analog-to-digital converter (ADC) and digital-to-analog converter (DAC) circuits, phase-locked loops (PLLs), voltage controlled oscillators (VCOs) and clocking integrated circuits
- Field programmable gate array (FPGA) and digital signal processor (DSP) supplies
- Medical and healthcare
- Industrial and instrumentation

GENERAL DESCRIPTION

The ADP1763 is a low noise, low dropout (LDO) linear regulator. It is designed to operate from a single input supply with an input voltage as low as 1.10 V without the requirement of external bias supply to increase efficiency and provide up to 3 A of output current.

The low 115 mV typical dropout voltage at a 3 A load allows the ADP1763 to operate with a small headroom while maintaining regulation and providing better efficiency.

The ADP1763 is optimized for stable operation with small 10 µF ceramic output capacitors. The ADP1763 delivers good transient performance with minimal board area.

TYPICAL APPLICATION CIRCUITS

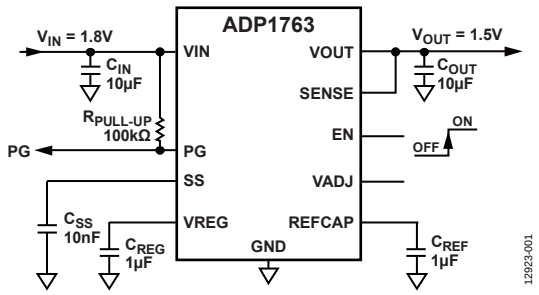

Figure 1. Fixed Output Operation

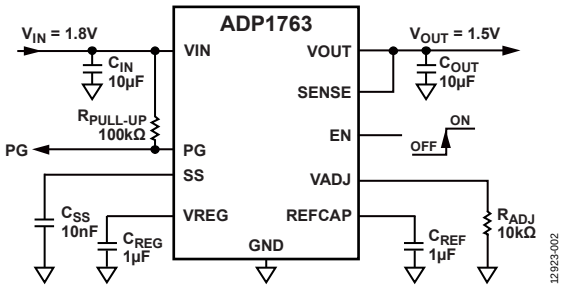

Figure 2. Adjustable Output Operation

Table 1. Related Devices

Model	Input Voltage	Maximum Current	Fixed/Adjustable	Package
ADP1761	1.10 V to 1.98 V	1 A	Fixed/adjustable	16-lead LFCSP
ADP1762	1.10 V to 1.98 V	2 A	Fixed/adjustable	16-lead LFCSP
ADP1740/ ADP1741	1.6 V to 3.6 V	2 A	Fixed/adjustable	16-lead LFCSP
ADP1752/ ADP1753	1.6 V to 3.6 V	0.8 A	Fixed/adjustable	16-lead LFCSP
ADP1754/ ADP1755	1.6 V to 3.6 V	1.2 A	Fixed/adjustable	16-lead LFCSP

The ADP1763 is available in fixed output voltages ranging from: 0.9 V to 1.5 V. The output of the adjustable output model can be set from 0.5 V to 1.5 V through an external resistor connected between VADJ and ground.

The ADP1763 has an externally programmable soft start time by connecting a capacitor to the SS pin. Short-circuit and thermal overload protection circuits prevent damage in adverse conditions. The ADP1763 is available in a small 16-lead LFCSP package for the smallest footprint solution to meet a variety of applications.

Rev. PrG Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

3/16—Revision PrG: Preliminary Version

SPECIFICATIONS

V_{IN} = V_{OUT} + 0.2 V or V_{IN} = 1.1 V, whichever is greater, I_{OUT} = 10 mA, C_{IN} = 10 µF, C_{OUT} = 10 µF, C_{REF} = 1 µF, C_{REG} = 1 µF, T_A = 25°C, Minimum and maximum limits at T_J = −40°C to +125°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE SUPPLY RANGE	V_{IN}	T_J = −40°C to +125°C	1.10		1.98	V
OPERATING SUPPLY CURRENT	I_{GND}	I_{OUT} = 0 µA		4.5	8	mA
		I_{OUT} = 10 mA		4.9	8	mA
		I_{OUT} = 100 mA		5.5	8.5	mA
		I_{OUT} = 3 A		12	16	mA
SHUTDOWN CURRENT	I_{GND-SD}	EN = GND		2		µA
		T_J = −40°C to +85°C, V_{IN} = V_{OUT} + 0.2 V to 1.98 V			180	µA
		T_J = 85°C to 125°C, V_{IN} = V_{OUT} + 0.2 V to 1.98 V			800	µA
OUTPUT NOISE	OUT_{NOISE}	10 Hz to 100 kHz, V_{IN} = 1.1 V, V_{OUT} = 0.9 V		12		µV rms
		100 Hz to 100 kHz, V_{IN} = 1.1 V, V_{OUT} = 0.9 V		2		µV rms
		10 Hz to 100 kHz, V_{IN} = 1.5 V, V_{OUT} = 1.3 V		15		µV rms
		100 Hz to 100 kHz, V_{IN} = 1.5 V, V_{OUT} = 1.3 V		2		µV rms
		10 Hz to 100 kHz, V_{IN} = 1.7 V, V_{OUT} = 1.5 V		21		µV rms
		100 Hz to 100 kHz, V_{IN} = 1.7 V, V_{OUT} =1.5 V		2		µV rms
Noise Spectral Density	OUT_{NSD}	V_{OUT} = 0.9 V to 1.5 V, I_{OUT} = 10 mA				
		At 10 kHz		4		nV/√Hz
		At 100 kHz		3		nV/√Hz
POWER SUPPLY REJECTION RATIO	PSRR	I_{OUT} = 3 A, modulated V_{IN}				
		10 kHz, V_{OUT} = 1.3 V, V_{IN} = 1.7 V		59		dB
		100 kHz, V_{OUT} = 1.3 V, V_{IN} = 1.7 V		43		dB
		1 MHz, V_{OUT} = 1.3 V, V_{IN} = 1.7 V		37		dB
		10 kHz, V_{OUT} = 0.9 V, V_{IN} = 1.3 V		62		dB
		100 kHz, V_{OUT} = 0.9 V, V_{IN} = 1.3 V		45		dB
		1 MHz, V_{OUT} = 0.9 V, V_{IN} = 1.3 V		33		dB
OUTPUT VOLTAGE RANGE		T_A = 25°C				
	V_{OUT_FIXED}		0.9		1.5	V
	V_{OUT_ADJ}		0.5		1.5	V
FIXED OUTPUT VOLTAGE ACCURACY	V_{OUT}	I_{OUT} = 100 mA, T_A = 25°C	−0.5		+0.5	%
		10 mA < I_{OUT} < 3 A, V_{IN} = (V_{OUT} + 0.2 V) to 1.98 V, T_J = 0°C to +85°C	−1		+1.5	%
		10 mA < I_{OUT} < 3 A, V_{IN} = (V_{OUT} + 0.2 V) to 1.98 V	−1.8		+1.5	%
ADJUSTABLE PIN CURRENT	I_{ADJ}	T_A = 25°C	49.5	50.0	50.5	µA
		V_{IN} = (V_{OUT} + 0.2 V) to 1.98 V	48.8	50.0	50.7	µA
ADJUSTABLE OUTPUT VOLTAGE GAIN FACTOR	A_D	T_A = 25°C		3.0		V
		V_{IN} = (V_{OUT} + 0.2 V) to 1.98 V	2.97		3.06	V
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = (V_{OUT} + 0.2 V) to 1.98 V	−0.15		+0.15	%/V
LOAD REGULATION[1]	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 10 mA to 3 A		0.12	0.35	%/A
DROPOUT VOLTAGE[2]	$V_{DROPOUT}$	I_{OUT} = 100 mA, V_{OUT} = 1.2 V		10	25	mV
		I_{OUT} = 3 A, V_{OUT} = 1.2 V		115	180	mV
START-UP TIME[3]	$T_{START-UP}$	C_{SS} = 10 nF, V_{OUT} = 1.3 V		0.6		ms
SOFT START CURRENT	I_{REF}	1.1 V ≤ V_{IN} ≤ 1.98 V	8	10	12	µA
CURRENT-LIMIT THRESHOLD[4]	I_{LIMIT}		3.3	4	5	A
THERMAL SHUTDOWN						
Threshold	TS_{SD}	T_J rising		150		°C
Hysteresis	TS_{SD-HYS}			15		°C

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
PGOOD OUTPUT THRESHOLD						
Output Voltage						
Falling	PG_{FALL}	$1.1\ V \le V_{IN} \le 1.98\ V$		−7.5		%
Rising	PG_{RISE}	$1.1\ V \le V_{IN} \le 1.98\ V$		−5		%
PGOOD (PG) OUTPUT						
Output Voltage Low	PG_{LOW}	$1.1\ V \le V_{IN} \le 1.98\ V$, $I_{PG} \le 1$ mA			0.35	V
Leakage Current	I_{PG-LKG}	$1.1\ V \le V_{IN} \le 1.98\ V$		0.01	1	µA
Delay	PG_{DELAY}	EN_{RISING} to PG_{RISING}		0.75		ms
PRECISION EN INPUT		$1.1\ V \le V_{IN} \le 1.98\ V$				
Logic Input						
High	EN_{HIGH}		0.60	0.63	0.68	V
Low	EN_{LOW}		0.55	0.58	0.63	V
Input Logic Hysteresis	EN_{HYS}			50		mV
Input Leakage Current	I_{EN-LKG}	$EN = V_{IN}$ or GND		0.01	1	µA
Input Delay Time	TI_{EN-DLY}	From EN rising from 0 V to V_{IN} to $0.1 \times V_{OUT}$		100		µs
UNDERVOLTAGE LOCKOUT	UVLO					
Input Voltage						
Rising	$UVLO_{RISE}$	$T_J = -40°C$ to $+125°C$		1.01	1.06	V
Falling	$UVLO_{FALL}$	$T_J = -40°C$ to $+125°C$	0.84	0.92		V
Hysteresis	$UVLO_{HYS}$			90		mV

[1] Based on an endpoint calculation using 1 mA and 3 A loads.
[2] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage, which applies only for output voltages above 1.1 V.
[3] Start-up time is defined as the time from the rising edge of EN to VOUT being at 90% of its nominal value.
[4] Current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 1.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 1.0 V, or 0.9 V.

INPUT AND OUTPUT CAPACITOR: RECOMMENDED SPECIFICATIONS

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CAPACITANCE[1]		$T_A = -40°C$ to $+125°C$				
Input	C_{IN}		7.0	10		µF
Output	C_{OUT}		7.0	10		µF
Regulator	C_{REG}		0.7	1		µF
Reference	C_{REF}		0.7	1		µF
CAPACITOR EQUIVALENT SERIES RESISTANCE (ESR)	R_{ESR}	$T_A = -40°C$ to $+125°C$				
C_{IN}, C_{OUT}			0.001		0.05	Ω
C_{REG}, C_{REF}			0.001		0.2	Ω

[1] The minimum input and output capacitance must be >7.0 µF over the full range of the operating conditions. Consider the full range of the operating conditions in the application during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended. Y5V and Z5U capacitors are not recommended for use with any LDO.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
VIN to GND	−0.3 V to +2.16 V
EN to GND	−0.3 V to +3.96 V
VOUT to GND	−0.3 V to VIN
SENSE to GND	−0.3 V to VIN
VREG to GND	−0.3 V to VIN
REFCAP to GND	−0.3 V to VIN
VADJ to GND	−0.3 V to VIN
SS to GND	−0.3 V to VIN
PG to GND	−0.3 V to +3.96 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Operating Junction Temperature	125°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL DATA

Absolute maximum ratings apply only individually, not in combination. The ADP1763 may be damaged when junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that the junction temperature is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may need to be derated.

In applications with moderate power dissipation and low printed circuit board (PCB) thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}). T_J is calculated using the following formula:

$$T_J = T_A + (P_D \times \theta_{JA})$$

The junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and a calculation using a 4-layer board.

The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. The specified values of θ_{JA} are based on a 4-layer, 4 in × 3 in circuit board. For details about board construction, refer to JEDEC JESD51-7.

Ψ_{JB} is the junction-to-board thermal characterization parameter with units of °C/W. Ψ_{JB} of the package is based on modeling and a calculation using a 4-layer board. The JEDEC JESD51-12 document, *Guidelines for Reporting and Using Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than a single path, as in thermal resistance (θ_{JB}). Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications. The maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D), using the following formula:

$$T_J = T_B + (P_D \times \Psi_{JB})$$

Refer to the JEDEC JESD51-8 and JESD51-12 documents for more detailed information about Ψ_{JB}.

THERMAL RESISTANCE

θ_{JA} and Ψ_{JB} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance for a 4-Layer 6400 mm² Copper Size

Package Type	θ_{JA}	Ψ_{JB}	Unit
16-Lead LFCSP	56	28.4	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

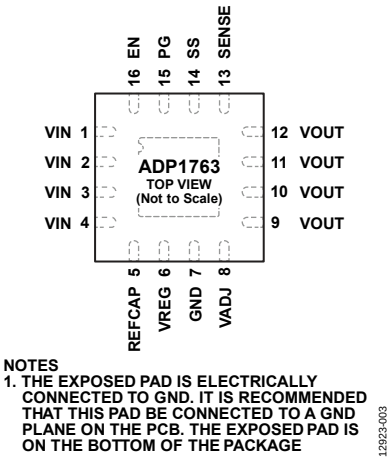

Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 4	VIN	Regulator Input Supply. Bypass VIN to GND with a 10 µF or greater capacitor. Note that all four VIN pins must be connected to the source supply.
5	REFCAP	Reference Filter Capacitor. Connect a 1 µF capacitor from REFCAP pin to ground. Do not connect a load to ground.
6	VREG	Regulated Input Supply to LDO Amplifier. Bypass VREG to GND with a 1 µF or greater capacitor. Do not connect a load to ground.
7	GND	Ground.
8	VADJ	Adjustable Voltage Pin for the Adjustable Output Option. Connect a 10 kΩ external resistor between the VADJ pin and ground to set the output voltage to 1.5 V. For the fixed output option, leave this pin floating
9 to 12	VOUT	Regulated Output Voltage. Bypass VOUT to GND with a 10 µF or greater capacitor. Note that all four VOUT pins must be connected to the load.
13	SENSE	Sense Input. The SENSE pin measures the actual output voltage at the load and feeds it to the error amplifier. Connect VSENSE as close to the load as possible to minimize the effect of IR drop between VOUT and the load.
14	SS	Soft Start Pin. A 10 nF capacitor connected to the SS pin and ground sets the start-up time to 0.6 ms.
15	PG	Power-Good Output. This open-drain output requires an external pull-up resistor. If the device is in shutdown mode, current-limit mode, or thermal shutdown mode, or if VOUT falls below 90% of the nominal output voltage, the PG pin immediately transitions low.
16	EN	Enable Input. Drive the EN pin high to turn on the regulator. Drive the EN pin low to turn off the regulator. For automatic startup, connect the EN pin to the VIN pin.
	EP	Exposed Pad. The exposed pad is electrically connected to GND. It is recommended that this pad be connected to a ground plane on the PCB. The exposed pad is on the bottom of the package.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 1.5 V, V_{OUT} = 1.3 V, T_A = 25°C, unless otherwise noted.

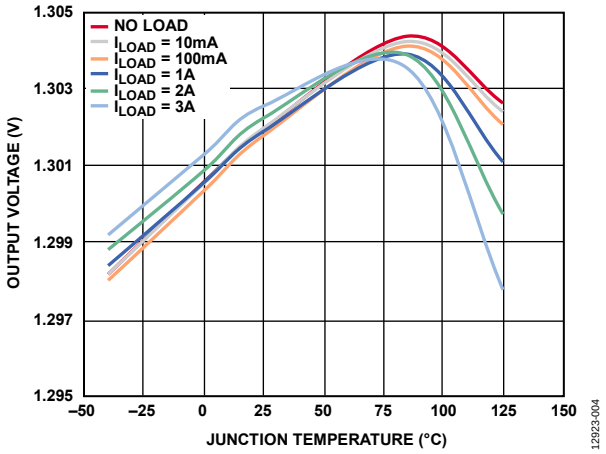

Figure 4. Output Voltage (V_{OUT}) vs. Junction Temperature

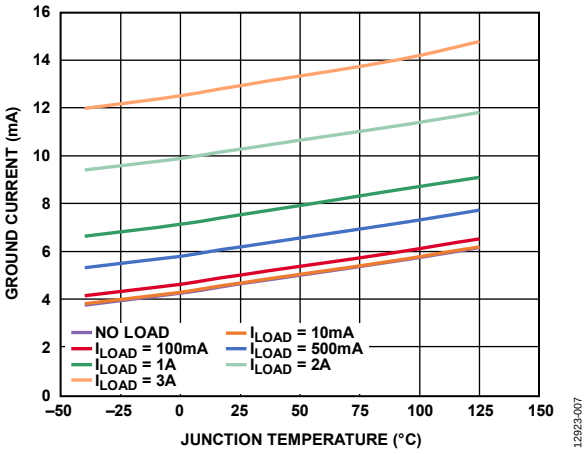

Figure 7. Ground Current vs. Junction Temperature

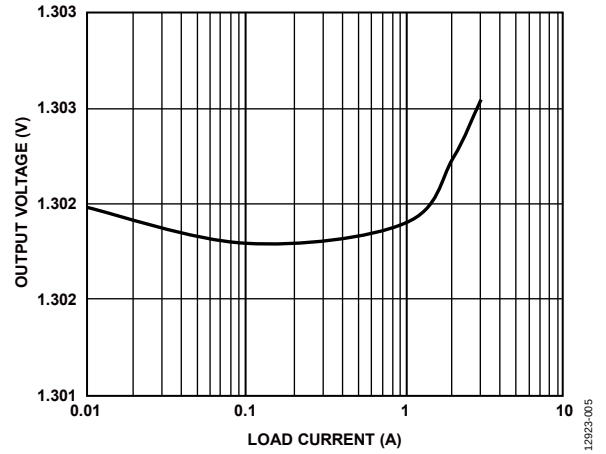

Figure 5. Output Voltage (V_{OUT}) vs. Load Current

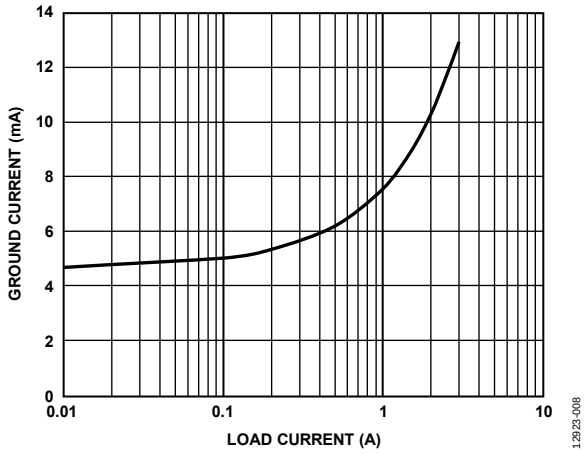

Figure 8. Ground Current vs. Load Current

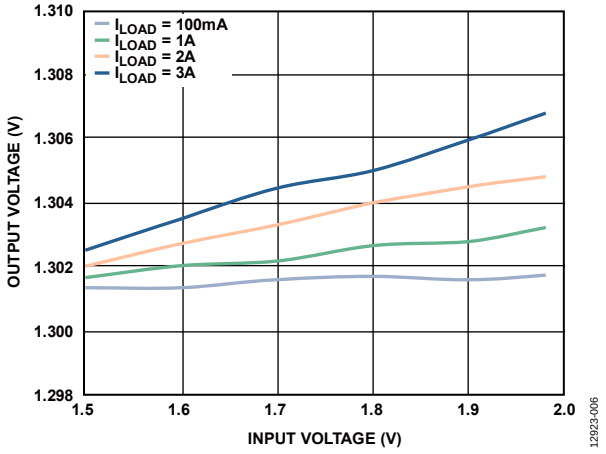

Figure 6. Output Voltage vs. Input Voltage

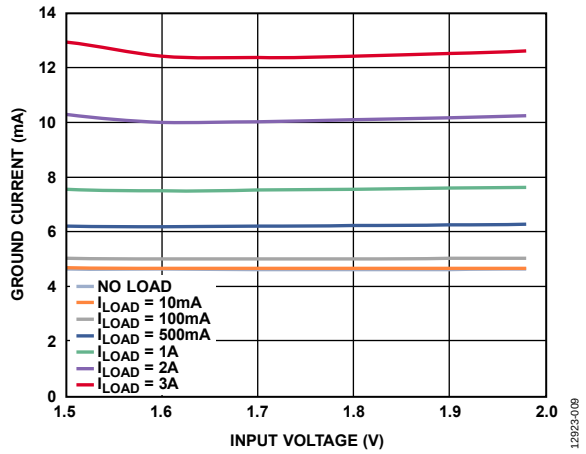

Figure 9. Ground Current vs. Input Voltage

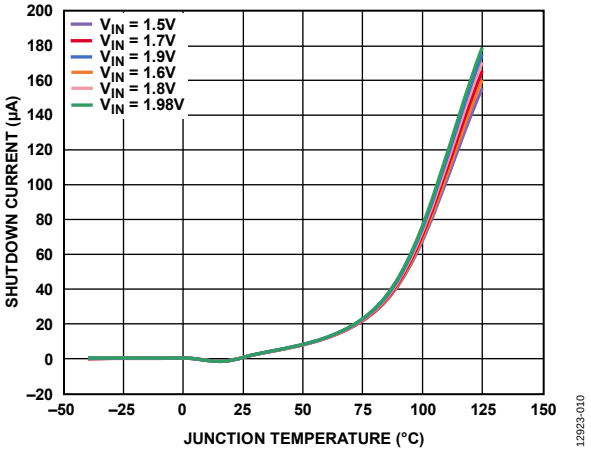

Figure 10. Shutdown Current vs. Junction Temperature at Various Input Voltages (V_{IN})

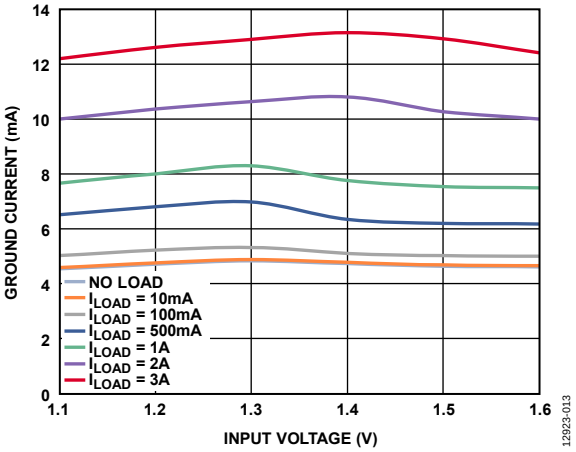

Figure 13. Ground Current vs. Input Voltage (in Dropout), V_{OUT} = 1.3 V

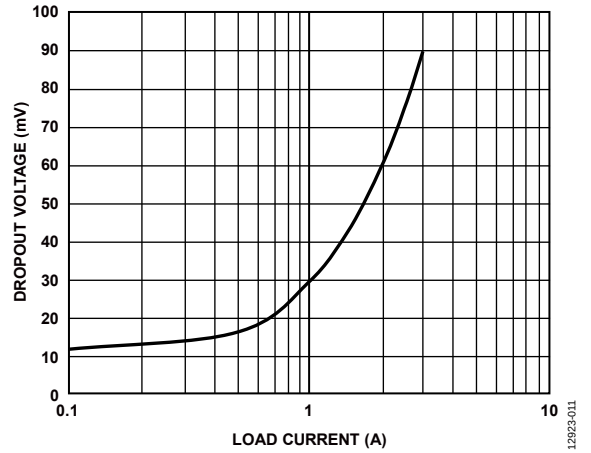

Figure 11. Dropout Voltage vs. Load Current, V_{OUT} = 1.3 V

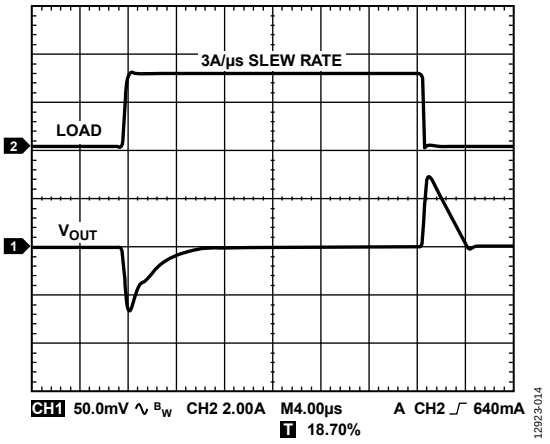

Figure 14. Load Transient Response, C_{OUT} = 10 µF, V_{IN} = 1.8 V, V_{OUT} = 1.3 V

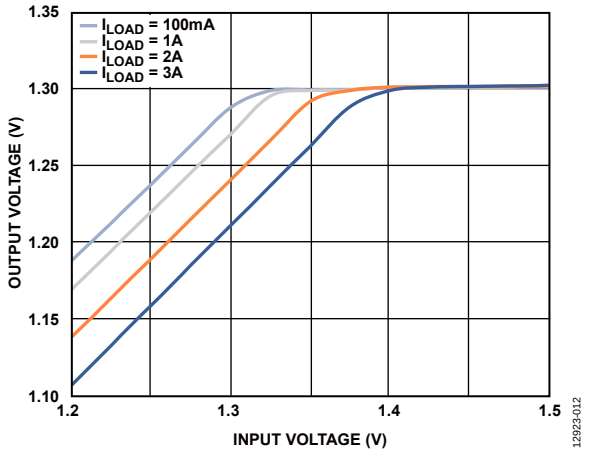

Figure 12. Output Voltage vs. Input Voltage (in Dropout), V_{OUT} = 1.3 V

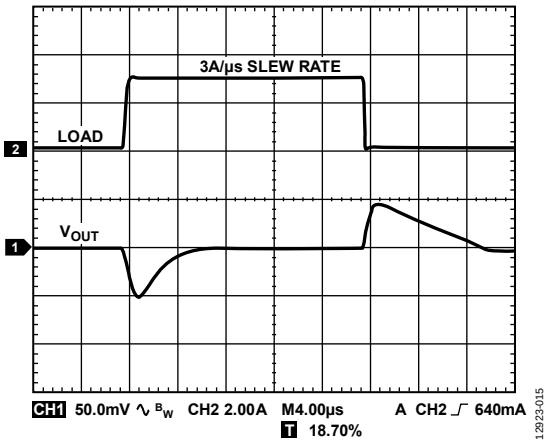

Figure 15. Load Transient Response, C_{OUT} = 47 µF, V_{IN} = 1.8 V, V_{OUT} = 1.3 V

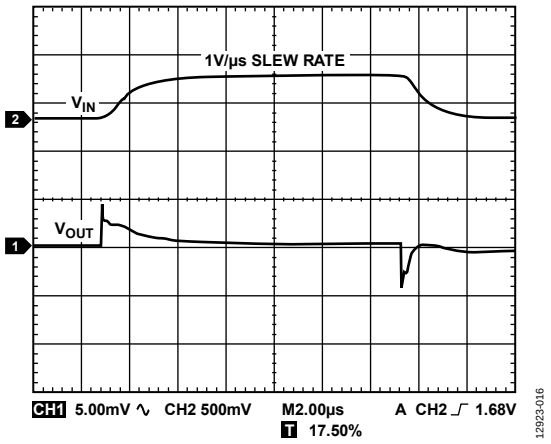

Figure 16. Line Transient Response, Load Current = 3 A, V_{IN} = 1.5 V to 1.98 V Step, V_{OUT} = 1.3 V

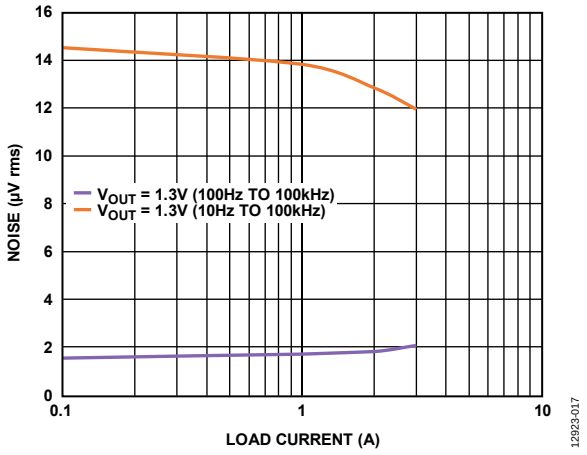

Figure 17. Noise vs. Load Current for Various Output Voltages

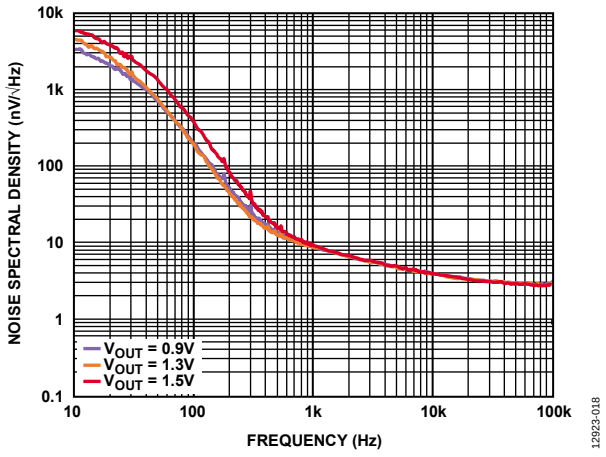

Figure 18. Noise Spectral Density vs. Frequency for Various Output Voltages, I_{LOAD} = 100 mA

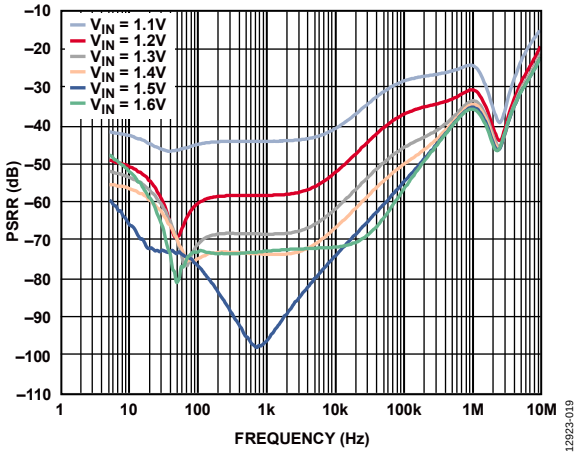

Figure 19. Power Supply Rejection Ratio (PSRR) vs. Frequency for Various Loads, V_{OUT} = 0.9 V, Load = 3 A

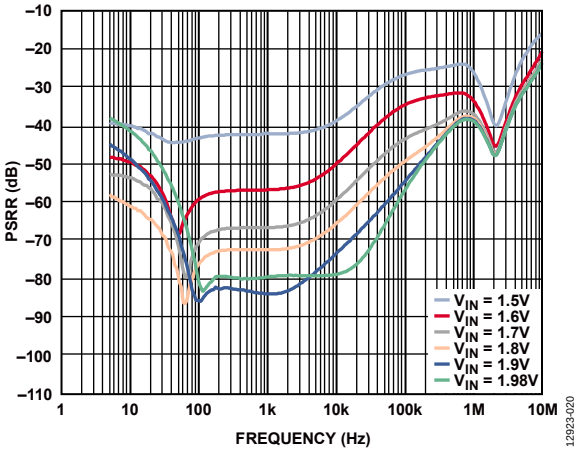

Figure 20. Power Supply Rejection Ratio (PSRR) vs. Frequency for Various Loads, V_{OUT} = 1.3 V, Load = 3 A

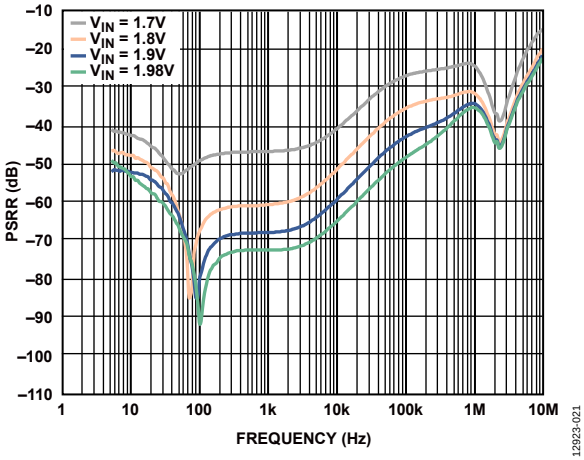

Figure 21. Power Supply Rejection Ratio (PSRR) vs. Frequency for Various Loads, V_{OUT} = 1.5 V, Load = 3 A

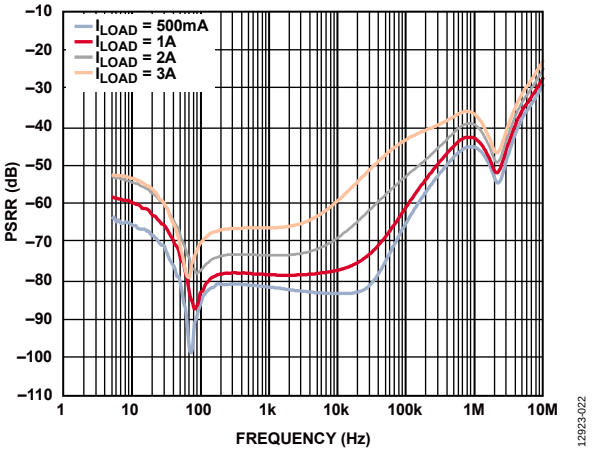

Figure 22. Power Supply Rejection Ratio (PSRR) vs. Frequency for Various Input Voltages, V_{OUT} = 1.3 V, V_{IN} = 1.7 V

THEORY OF OPERATION

The ADP1763 is a low dropout (LDO), low noise linear regulator that uses an advanced proprietary architecture to achieve high efficiency regulation. It also provides high power supply rejection ratio (PSRR) and excellent line and load transient response using a small 10 µF ceramic output capacitor. The device operates from a 1.10 V to 1.98 V input rail to provide up to 3 A of output current. Supply current in shutdown mode is less than 2 µA.

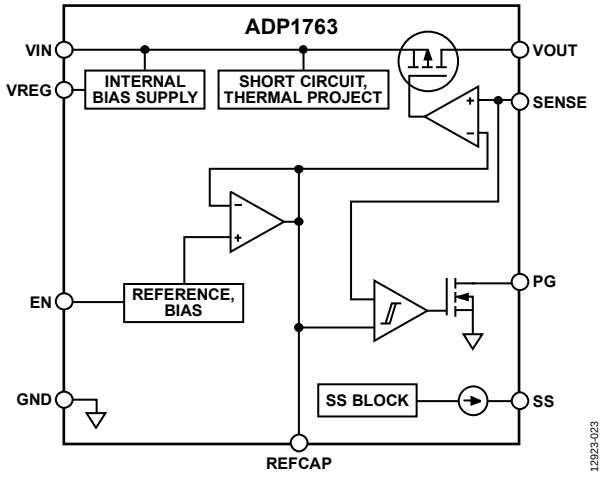

Figure 23. Functional Block Diagram, Fixed Output

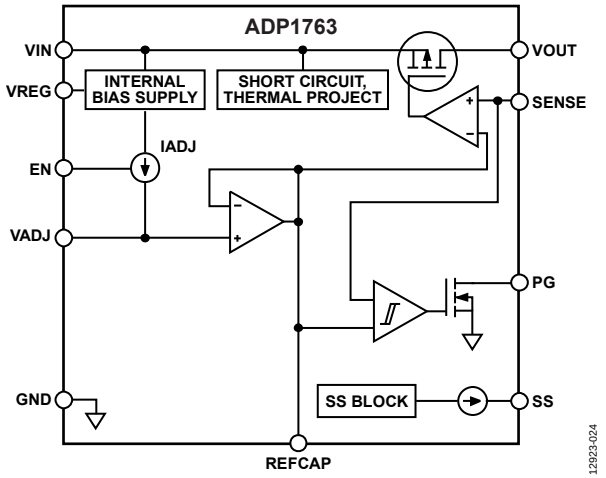

Figure 24. Functional Block Diagram, Adjustable Output

Internally, the ADP1763 consists of a reference, an error amplifier, and a pass device. The output current is delivered via the pass device, which is controlled by the error amplifier, forming a negative feedback system that ideally drives the feedback voltage to equal the reference voltage. If the feedback voltage is lower than the reference voltage, the negative feedback drives more current, increasing the output voltage. If the feedback voltage is higher than the reference voltage, the negative feedback drives less current, decreasing the output voltage.

The ADP1763 is available in output voltages ranging from 0.9 V to 1.5 V for a fixed output. Contact your local Analog Devices, Inc., sales representative for other fixed voltage options. The adjustable output option can be set from 0.5 V to 1.5 V. The ADP1763 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. When EN is high, VOUT turns on. When EN is low, VOUT turns off. For automatic startup, EN can be tied to VIN.

SOFT START FUNCTION

For applications that require a controlled startup, the ADP1763 provides a programmable soft start function. The programmable soft start is useful for reducing inrush current upon startup and for providing voltage sequencing. To implement soft start, connect a small ceramic capacitor from SS to GND. At startup, a 10 µA current source charges this capacitor. The voltage at SS limits the ADP1763 start-up output voltage, providing a smooth ramp up to the nominal output voltage. To calculate the start-up time for the fixed output and adjustable output, use the following equations:

$$T_{START\text{-}UP\_FIXED} = T_{DELAY} + V_{REF} \times (C_{SS}/I_{SS}) \quad (1)$$

$$T_{START\text{-}UP\_ADJ} = T_{DELAY} + V_{ADJ} \times (C_{SS}/I_{SS}) \quad (2)$$

where:

T_{DELAY} is a fixed delay of 100 µs.
V_{REF} is a 0.5 V internal reference for the fixed output model option.
C_{SS} is the soft start capacitance from SS to GND.
I_{SS} is the current sourced from SS (10 µA).
V_{ADJ} is the voltage at the VADJ pin equal to $R_{ADJ} \times I_{ADJ}$.

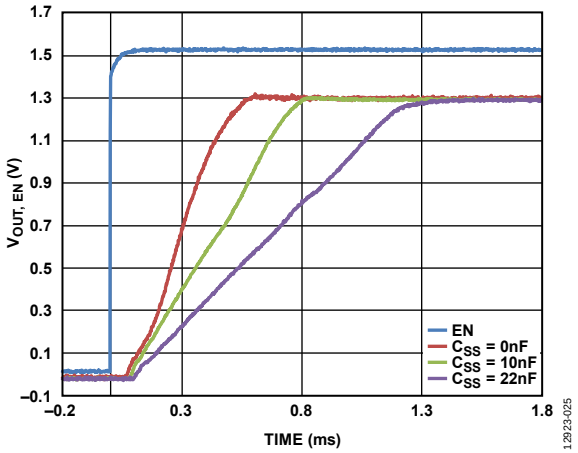

Figure 25. Fixed V_{OUT} Ramp-Up with External Soft Start Capacitor ($V_{OUT,EN}$) vs. Time

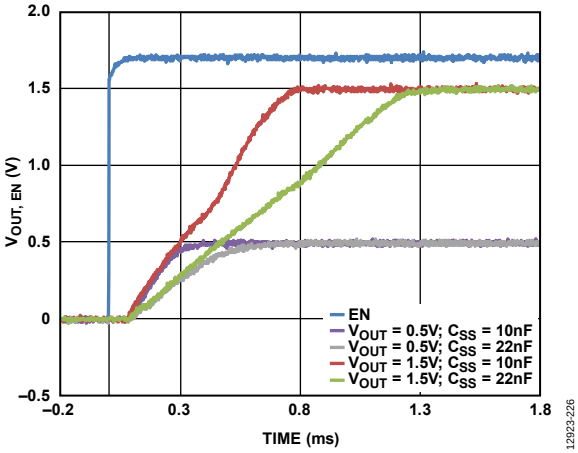

Figure 26. Adjustable V_{OUT} Ramp-Up with External Soft Start Capacitor ($V_{OUT,EN}$) vs. Time ($V_{OUT,EN}$) vs. Time

ADJUSTABLE OUTPUT VOLTAGE

The output voltage of the ADP1763 can be set over a 0.5 V to 1.5 V range. Connect a resistor (R_{ADJ}) from the VADJ pin to ground to set the output voltage. To calculate the output voltage, use the following equation:

$$V_{OUT} = A_D \times (R_{ADJ} \times I_{ADJ}) \quad (3)$$

where:

A_D is the gain factor with a typical value of 3 between the VADJ pin and VOUT pin.

I_{ADJ} is the 50 µA constant current out of the VADJ pin.

ENABLE FEATURE

The ADP1763 uses the EN pin to enable and disable the VOUT pins under normal operating conditions. As shown in Figure 27, when a rising voltage on EN crosses the active threshold, VOUT turns on. When a falling voltage on EN crosses the inactive threshold, VOUT turns off.

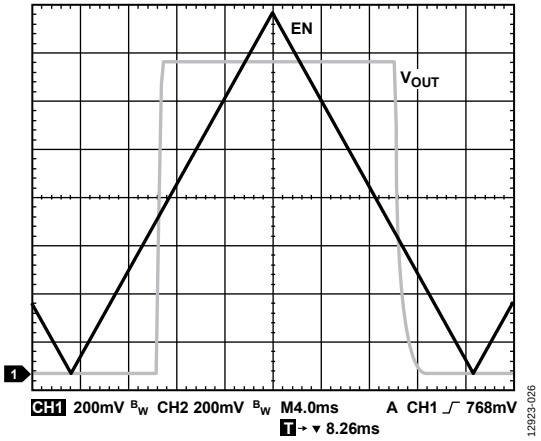

Figure 27. Typical EN Pin Operation

As shown in Figure 28, the EN pin has hysteresis built in. This hysteresis prevents on/off oscillations that can occur due to noise on the EN pin as it passes through the threshold points.

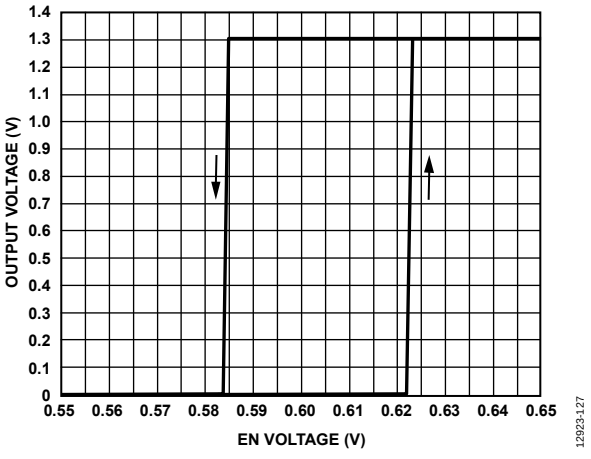

Figure 28. Typical EN Pin Thresholds vs. Output Voltage, V_{OUT} = 1.3 V

POWER-GOOD (PG) FEATURE

The ADP1763 provides a power good pin (PG) to indicate the status of the output. This open-drain output requires an external pull-up resistor that can be connected to V_{IN} or V_{OUT}. If the device is in shutdown mode, current-limit mode, or thermal shutdown, or if it falls below 90% of the nominal output voltage, PG immediately transitions low. During soft start, the rising threshold of the power good signal is 95% of the nominal output voltage.

The open-drain output is held low when the ADP1763 have sufficient input voltage to turn on the internal PG transistor. An optional soft start delay can be detected. The PG transistor is terminated via a pull-up resistor to V_{OUT} or V_{IN}.

Power-good accuracy is 92.5% of the nominal regulator output voltage when this voltage is rising, with a 95% trip point when this voltage is falling.

Regulator input voltage brownouts or glitches trigger a power no good if V_{OUT} falls below 92.5%.

A normal power-down triggers a power good when V_{OUT} is at 95%.

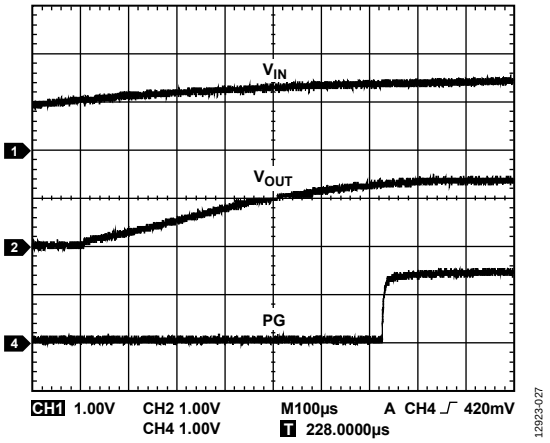

Figure 29. Typical PG Behavior vs. V_{OUT}, V_{IN} Rising (V_{OUT} = 1.3 V)

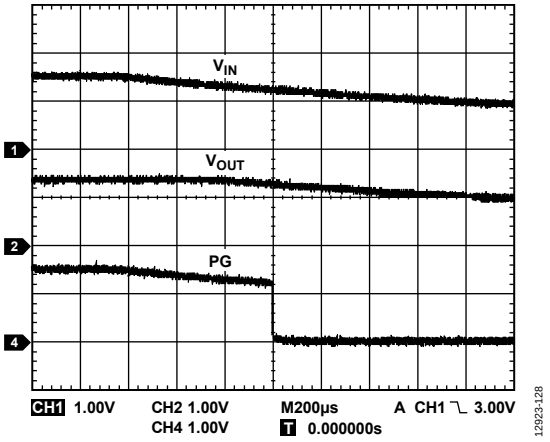

Figure 30. Typical PG Behavior vs. V_{OUT}, V_{IN} Falling (V_{OUT} = 1.3 V)

APPLICATIONS INFORMATION

CAPACITOR SELECTION

Output Capacitor

The ADP1763 is designed for operation with small, space-saving ceramic capacitors, but they can function with most commonly used capacitors as long as care is taken with the effective series resistance (ESR) value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 10 µF capacitance with an ESR of 500 mΩ or less is recommended to ensure the stability of the ADP1763. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP1763 to large changes in load current. Figure 31 and Figure 32 show the transient responses for output capacitance values of 10 µF and 47 µF, respectively.

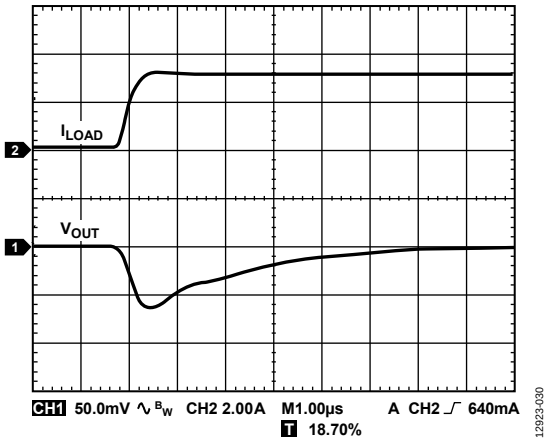

Figure 31. Output Transient Response, C_{OUT} = 10 µF

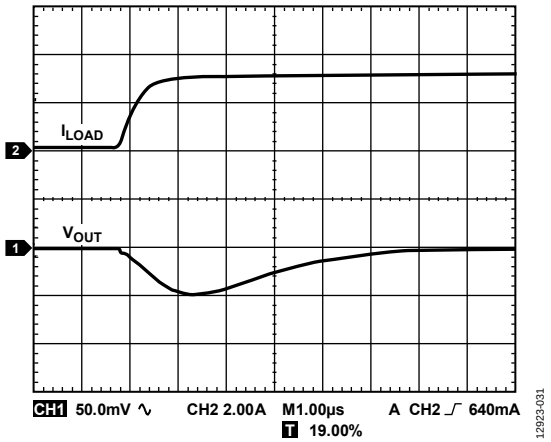

Figure 32. Output Transient Response, C_{OUT} = 47 µF

Input Bypass Capacitor

Connecting a 10 µF capacitor from the VIN pin to GND pin to ground reduces the circuit sensitivity to the PCB layout, especially when long input traces or high source impedance are encountered. If output capacitance greater than 10 µF is required, it is recommended that the input capacitor be increased to match it.

Input and Output Capacitor Properties

Use any good quality ceramic capacitors with the ADP1763, as long as they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended. Y5V and Z5U dielectrics are not recommended, due to their poor temperature and dc bias characteristics.

Figure 33 shows the capacitance vs. bias voltage characteristics of an 0805 case, 10 µF, 10 V, X5R capacitor. The voltage stability of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or with a higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is about ±15% over the −40°C to +85°C temperature range and is not a function of package size or voltage rating.

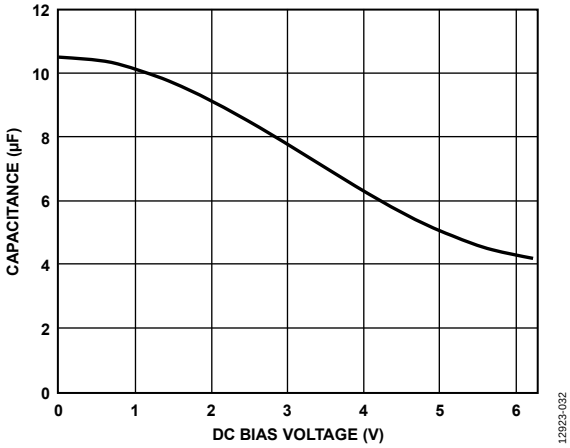

Figure 33. Capacitance vs. DC Bias Voltage

Use Equation 4 to determine the worst-case capacitance, accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{OUT} \times (1 - TEMPCO) \times (1 - TOL) \quad (4)$$

where:
C_{EFF} is the effective capacitance at the operating voltage.
C_{OUT} is the output capacitor.
TEMPCO is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{OUT} = 10 µF at 1.0 V, as shown in Figure 33.

Substituting these values in Equation 4 yields

$$C_{EFF} = 10\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 7.65\ \mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADP1763, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

UNDERVOLTAGE LOCKOUT

The ADP1763 have an internal undervoltage lockout circuit that disables all inputs and the output when the input voltage is less than approximately 1.05 V. The UVLO ensures that the ADP1763 inputs and the output behave in a predictable manner during power-up.

CURRENT-LIMIT AND THERMAL OVERLOAD PROTECTION

The ADP1763 is protected against damage due to excessive power dissipation by current-limit and thermal overload protection circuits. The ADP1763 is designed to reach current limit when the output load reaches 4 A (typical). When the output load exceeds 4 A, the output voltage is reduced to maintain a constant current limit.

Thermal overload protection is included, which limits the junction temperature to a maximum of 150°C (typical). Under extreme conditions (that is, high ambient temperature and power dissipation) when the junction temperature begins to rise above 150°C, the output is turned off, reducing the output current to zero. When the junction temperature drops below 135°C (typical), the output is turned on again, and the output current is restored to its nominal value.

Consider the case where a hard short from VOUT to ground occurs. At first, the ADP1763 reaches current limit so that only 4 A is conducted into the short. If self-heating of the junction becomes great enough to cause its temperature to rise above 150°C, thermal shutdown activates, turning off the output and reducing the output current to zero. As the junction temperature cools and drops below 135°C, the output turns on and conducts 4 A into the short, again causing the junction temperature to rise above 150°C. This thermal oscillation between 135°C and 150°C causes a current oscillation between 4 A and 0 A that continues as long as the short remains at the output.

Current-limit and thermal overload protections are intended to protect the device against accidental overload conditions. For reliable operation, device power dissipation should be externally limited so that junction temperatures do not exceed 125°C.

PARALLELING ADP1763 FOR HIGH CURRENT APPLICATION

In applications where high output current is required while maintaining low noise and high PSRR performance, connect two ADP1763 devices in parallel to handle loads up to 5 A.

When paralleling the ADP1763, the two outputs must be of the same voltage setting to maintain good current sharing between the two LDOs. To improve current sharing accuracy, add identical ballast resistors ($R_{BALLAST}$) at the output of each regulator, as shown in Figure 34. Note that large ballast resistors improve current sharing accuracy but degrade the load regulation performance and increase the losses along the power line; therefore, it is still best to keep the ballast resistors at a minimum. In addition, tie the VADJ, SS, and REFCAP pins of the LDO regulators together to minimize error between the two outputs.

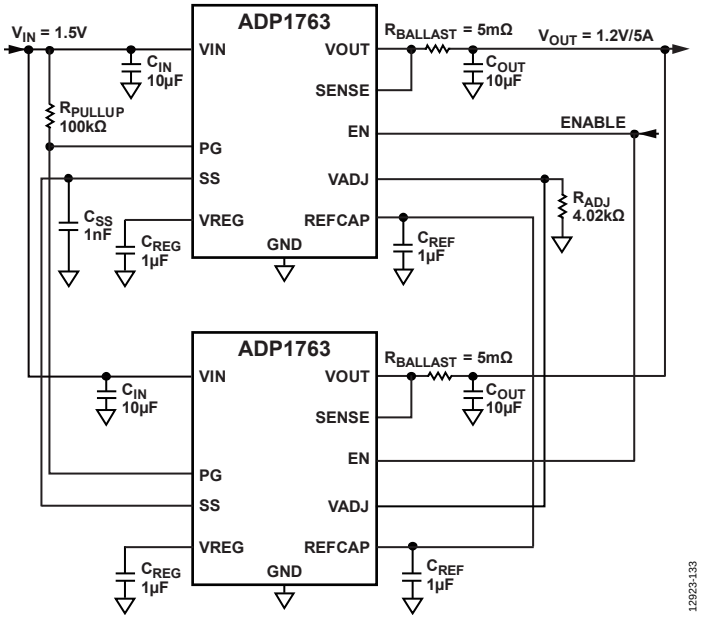

Figure 34. Two ADP1763 Devices Connected in Parallel to Achieve Higher Current Output

Use Equation 5 to calculate the output of the two paralleled ADP1763 LDOs.

$$V_{OUT} = 2 \times A_D \times (R_{ADJ} \times I_{ADJ}) \quad (5)$$

where:
A_D is the gain factor with a typical value of 3 between the VADJ pin and VOUT pin.
I_{ADJ} is the 50 µA constant current out of the VADJ pin.

THERMAL CONSIDERATIONS

To guarantee reliable operation, the junction temperature of the ADP1763 must not exceed 125°C. To ensure that the junction temperature stays below this maximum value, the user needs to be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistance between the junction and ambient air (θ_{JA}). The θ_{JA} value is dependent on the package assembly compounds used and the amount of copper to which the GND pin and the exposed pad (EPAD) of the package are soldered on the PCB. Table 7 shows typical θ_{JA} values for the 16-lead LFCSP for various PCB copper sizes. Table 8 shows typical Ψ_{JB} values for the 16-lead LFCSP.

Table 7. Typical θ_{JA} Values

Copper Size (mm²)	θ_{JA} (°C/W), LFCSP
25	138.1
100	102.9
500	76.9
1000	67.3
6400	56

Table 8. Typical Ψ_{JB} Values

Copper Size (mm²)	Ψ_{JB} (°C/W) at 1 W
100	33.3
500	28.9
1000	28.5

To calculate the junction temperature of the ADP1763, use the following equation:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (6)$$

where:
T_A is the ambient temperature.
P_D is the power dissipation in the die, given by

$$P_D = [(V_{IN} - V_{OUT}) \times I_{LOAD}] + (V_{IN} \times I_{GND}) \quad (7)$$

where:
V_{IN} and V_{OUT} are the input and output voltages, respectively.
I_{LOAD} is the load current.
I_{GND} is the ground current.

As shown in Equation 6, for a given ambient temperature, and computed power dissipation, a minimum copper size requirement exists for the PCB to ensure that the junction temperature does not rise above 125°C.

Figure 35 through Figure 40 show junction temperature calculations for different ambient temperatures, load currents, V_{IN} to V_{OUT} differentials, and areas of PCB copper.

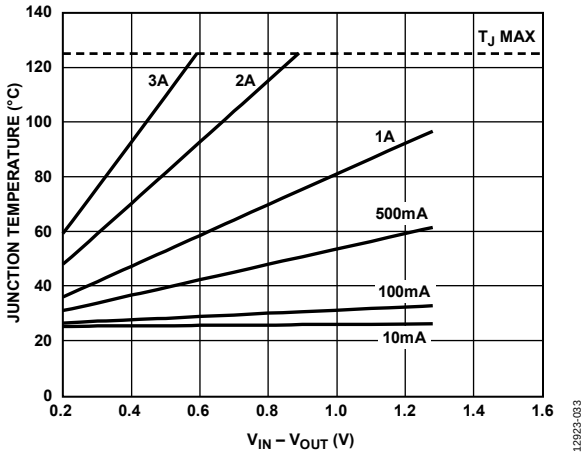

Figure 35. 6400 mm² of PCB Copper, T_A = 25°C, LFCSP

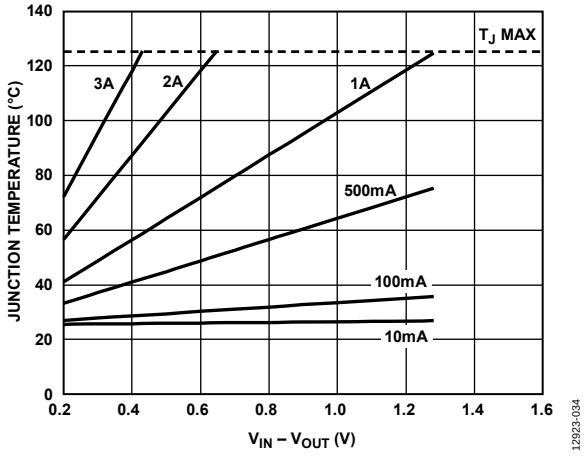

Figure 36. 500 mm² of PCB Copper, T_A = 25°C, LFCSP

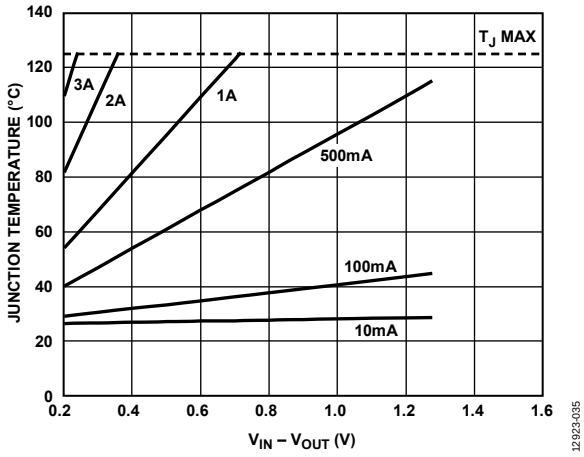

Figure 37. 25 mm² of PCB Copper, T_A = 25°C, LFCSP

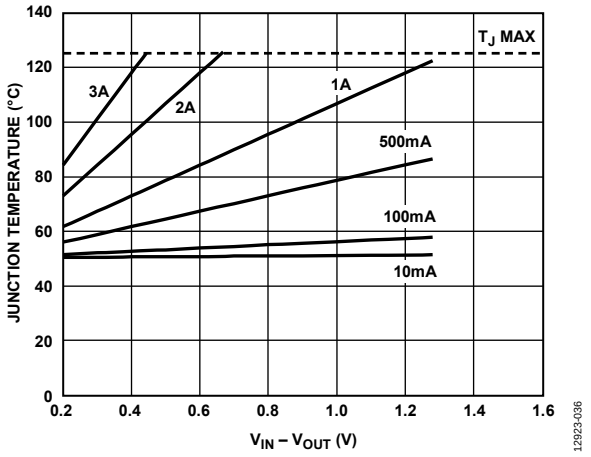

Figure 38. 6400 mm² of PCB Copper, T_A = 50°C, LFCSP

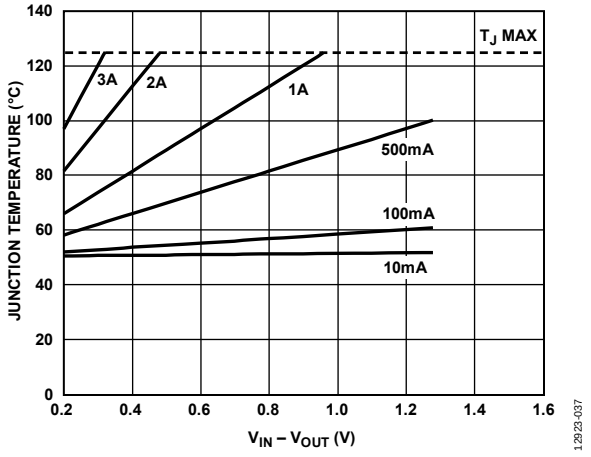

Figure 39. 500 mm² of PCB Copper, T_A = 50°C, LFCSP

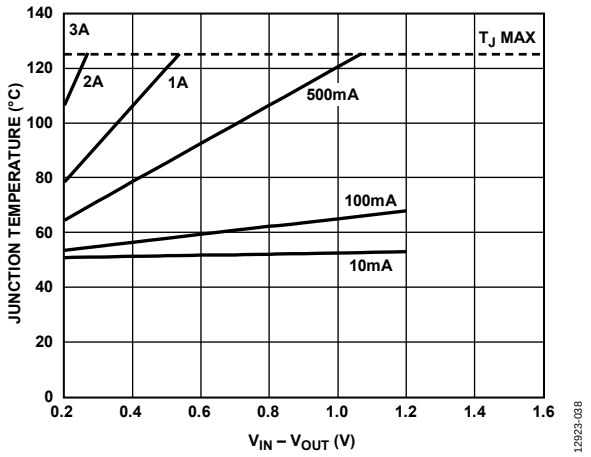

Figure 40. 25 mm² of PCB Copper, T_A = 50°C, LFCSP

In cases where the board temperature is known, the thermal characterization parameter (Ψ_{JB}) can be used to estimate the junction temperature rise. The maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the following formula:

$$T_J = T_B + (P_D \times \Psi_{JB}) \quad (8)$$

Figure 41 through Figure 44 show junction temperature calculations for different board temperatures, load currents, V_{IN} to V_{OUT} differentials, and areas of PCB copper.

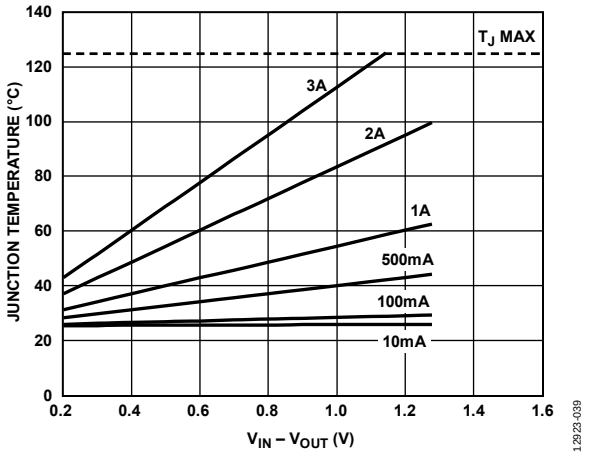

Figure 41. 500 mm² of PCB Copper, T_B = 25°C, LFCSP

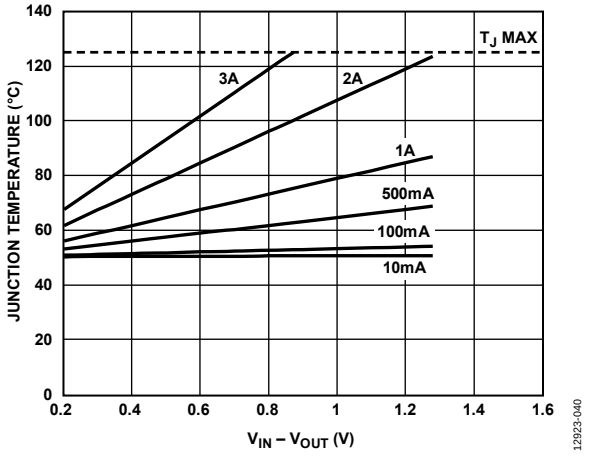

Figure 42. 500 mm² of PCB Copper, T_B = 50°C, LFCSP

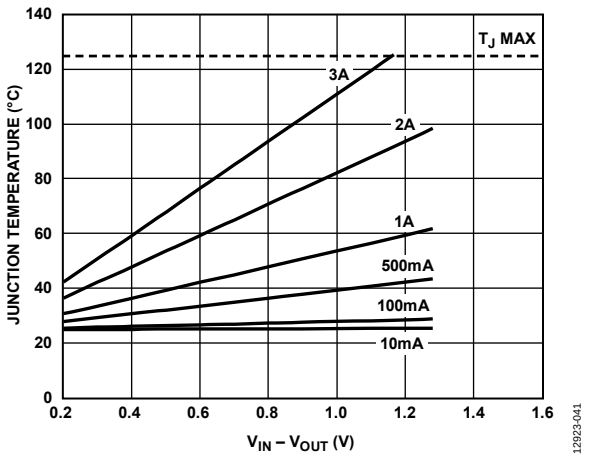

Figure 43. 1000 mm² of PCB Copper, T_B = 25°C, LFCSP

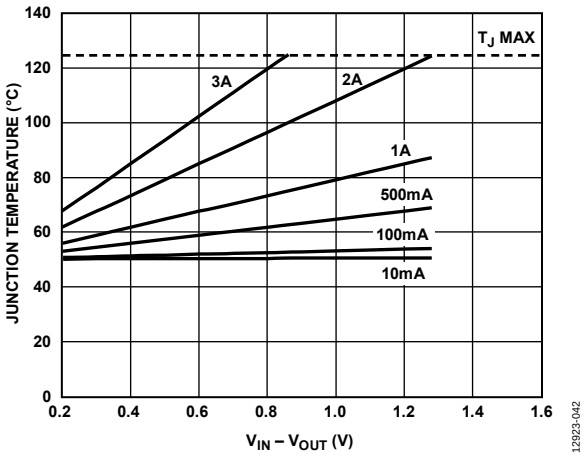

Figure 44. 1000 mm² of PCB Copper, T_B = 50°C, LFCSP

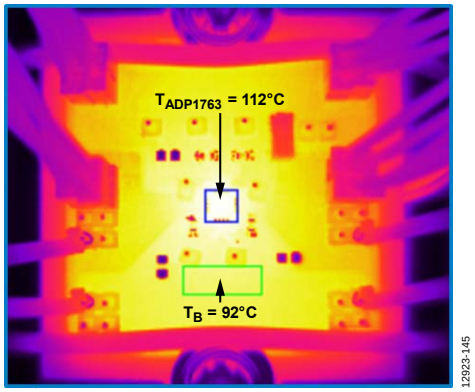

Figure 45. Thermal Image of the ADP1763 Evaluation Board at I_{LOAD} = 3 A, V_{IN} = 1.5 V, V_{OUT} = 1.3 V, T_B = 92°C

Figure 45 shows a thermal image of the ADP1763 evaluation board operating at a 3 A load. The total power dissipation on the ADP1763 is 600 mW which makes the temperature on the surface of the device higher by 30°C than the temperature of the evaluation board.

PCB LAYOUT CONSIDERATIONS

Heat dissipation from the package can be improved by increasing the amount of copper attached to the pins of ADP1763. However, as shown in Table 8, a point of diminishing returns is eventually reached, beyond which an increase in the copper size does not yield significant heat dissipation benefits.

Here are a few general tips when designing PCBs:

- Place the input capacitor as close as possible to the VIN and GND pins.
- Place the output capacitor as close as possible to the VOUT and GND pins.
- Place the soft start capacitor (C_{SS}) as close as possible to the SS pin.
- Place the reference capacitor (C_{REF}) and regulator capacitor (C_{REG}) as close as possible to the REFCAP pin and VREG pin, respectively.
- Connect the load as close as possible to the VOUT and SENSE pins.

Use of 0603 or 0805 size capacitors and resistors achieves the smallest possible footprint solution on boards where area is limited.

Figure 46. Evaluation Board

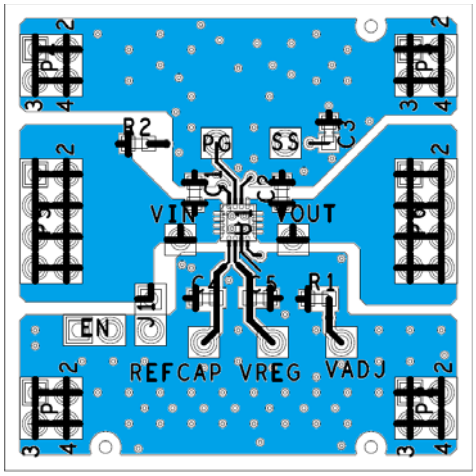

Figure 47. Typical Board Layout, Top Side

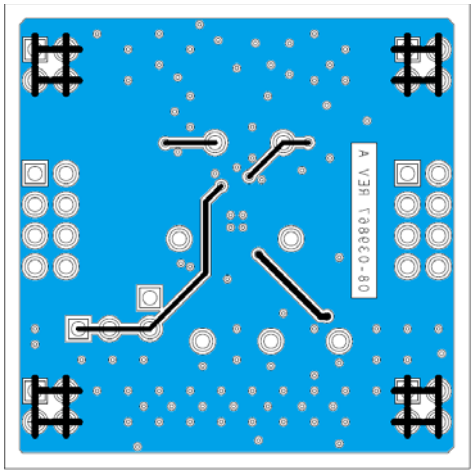

Figure 48. Typical Board Layout, Bottom Side

OUTLINE DIMENSIONS

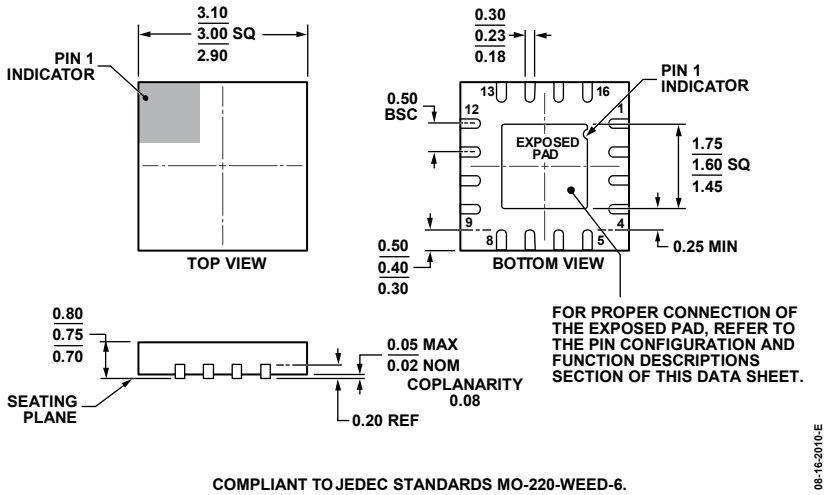

Figure 49. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-16-22)
Dimensions shown in millimeters

PR12923-0-3/16(PrG)